31.7 A Bandpass ΔΣ RF-DAC with Embedded FIR Reconstruction Filter

Shahin Mehdizad Taleie, Tino Copani, Bertan Bakkaloglu, Sayfe Kiaei

Arizona State University, Tempe, AZ

Current-steering DAC architectures provide fast-settling and high-dynamic-range performance, making them suitable for high-frequency applications including direct digital synthesizers, measurement instruments, and broadband communication circuits. However, their SFDR performance can be limited by the unit current source mismatch, finite output impedance, update clock jitter, and data dependent glitches at the current sources, most of which degrade with increased clock frequency [1]. In this paper, a 1b bandpass ΔΣ DAC that is followed by a current-steering FIR reconstruction filter with an embedded up-conversion mixer is presented. The DAC allows digital IF up-conversion, reducing LO leakage and I/Q mismatch, suitable for low-power software-defined digital-IF transmitter ICs. Digital ΔΣ noise-shaped DACs provide high-SFDR performance with reduced dependency on unit current source matching. In a typical digital transmitter, a current-steering DAC is followed by a transimpedance stage, a reconstruction filter, a VGA, and an up-converting mixer. Addition of each component degrades the linearity, I/Q matching, EVM, and SFDR [2].

The architecture of the 1b bandpass ΔΣ DAC is shown in Fig. 31.7.1. Digital-IF signal is generated by a direct-digital frequency synthesizer (DDFS) followed by a 2nd-order bandpass ΔΣ modulator with noise transfer function centered at $f_s/4$. IF clock phase noise coming from DDFS can convolve with the out-of-band quantization noise of the IF bitstream and increase in-band SNR of the RF output. Therefore, the 1b output of the bandpass ΔΣ modulator is re-sampled by a low-noise IF clock. The IF data and buffered clock lines drive a 6-tap digital delay line. The outputs of the delay line are connected to cascoded NMOS switching pairs forming a current-mode semi-digital FIR filter.

Circuit-level implementation of a unit FIR tap is shown in Fig. 31.7.2. The LO signal with a programmable dc-bias level controls the rail current source bias. The LO dc-bias level is controlled with a level-shifting amplifier. The RF DAC also has a programmable phase delay between the RF LO and bandpass IF bitstream to ensure precise phase relationship between the LO transitions with respect to IF update clock. Rise and fall time mismatches and glitch energy at IF data transitions can fold the out-of-band quantization-noise energy and spurs into signal band, reducing the in-band SFDR. By phase aligning LO nulls to IF clock transitions, signal dependent glitches at the IF output are minimized.

The design of the reconstruction filter at the discrete-time to continuous-time boundary can be greatly simplified by using a multi-bit input bitstream. However, the reconstruction filter linearity have to meet the overall transmitter 3rd-order intermodulation (IM3) requirement; this requires the use of dynamic element-matching circuitry operating at the IF frequency. Furthermore, multi-bit FIR filter coefficients increase the number of current sources connected to the LO buffers. By utilizing 1b configuration, the complexity and the coefficient mismatch requirements of the DAC can be relaxed. On the other hand, 1b DAC has higher out-of-band quantization noise and it is more prone to the IF signal transitions and clock jitter. In the proposed architecture, the IF signal transition phase noise impact is minimized by appropriate LO phase alignment. The zero locations of the FIR filter can be programmed by modifying the LO-to-IF frequency divider. Figure 31.7.3 shows the FIR filter response for f_s=125MHz, where the quantization noise is significantly suppressed at the adjacent channels.

To up-convert the signal to RF, the RF DAC tail current sources are switched by the LO signal. By combining the mixing operation at the DAC bias, there is no need for a stand-alone mixer, reducing the power consumption, area, and more significantly, the noise generated by the mixer. Overall linearity of the transmitter is also greatly increased. In a typical Gilbert mixer the linearity is limited by the IF input transistors and the NF of the mixer is well over 7dB. In this approach, a bandpass modulated rail-to-rail IF signal is utilized for switching the pass transistors between triode and cutoff regions yielding excellent intermodulation performance compared to a DAC followed by a Gilbert-cell mixer.

The proposed embedded mixer modulates the rail device between strong inversion and accumulation modes. This switching technique reduces the impact of the unit current source flicker noise on the output spectrum, reducing the up-converted 1/f noise sidebands around the output RF signal [3]. Since flicker noise depends on the device gate area with this technique unit current source device sizes can be reduced without increasing the gate area. This area reduction reduces parasitic capacitance seen by the LO buffers, adding flexibility for using higher number of taps and reducing power consumption. A similar bias switching technique is used in an RF DAC architecture for unit element biasing [4]. In the proposed topology, the bias lines for a semi-digital reconstruction filter coefficients are modulated.

As shown in Fig. 31.7.2, the LO driver calibrates the LO amplitude and its dc bias. By lowering the LO dc level, the up-converted flicker noise sidebands are reduced, however, this also reduces the output signal power. An optimum dc level can be selected based on the output signal power and the close-in phase noise specifications.

The 6-tap FIR DAC is realized using a 0.25μm digital CMOS process. The FIR DAC including the LO buffers, clock dividers, and calibration circuits occupies 0.23mm^2 area and consumes 122mW power from a 2.5V supply at 1GHz LO and 125MHz clock. Figure 31.7.4 shows the measured output spectrum of the up-converted channel centered at 1.031GHz with filtered quantization noise. Figure 31.7.5 shows the in-band SNR and SFDR of the up-converted spectrum for LO frequencies of 800MHz, 900MHz, and 1GHz for various integration bandwidths. The DAC achieves an SFDR of 72dB at 1.032GHz output for a frequency band of 15MHz. Figure 31.7.6 shows the two-tone intermodulation performance for f_{LO}=1GHz, f_s=125MHz, with f_1=31.5MHz and f_2=32.2MHz. The DAC achieves an IM3 of -64.7dBc at 1.032GHz output frequency. The die micrograph of the system is shown in Figure 31.1.7.

Acknowledgements:
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References:
[1] W. Schofield et al., "A 16b 400MS/s DAC with <-80dBc IMD to 300MHz and <-160dBm/Hz Noise Power Spectral Density," *ISSCC Dig. Tech. Papers*, pp. 126-127, Feb., 2003.
[2] V. W. Leung, L. E. Larson, P. S. Gudem, "Digital-IF WCDMA Handset Transmitter IC in 0.25μm SiGe BiCMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2215-2225, Dec., 2005.
[3] A. P. van der Wel, E. A. M Klumperink, B. Nauta, "Effect of Switched Biasing on 1/f Noise and Random Telegraph Signals in Deep-Submicron MOSFETs," Electronics Letters, vol. 37, no 1, pp. 55 – 56, Jan., 2001.
[4] S. Luschas, R. Schreier, H-S Lee, "Radio Frequency D/A Converter," *IEEE J. of Solid-State Circuits*, vol. 39, no. 9, pp. 1462-1467, Sept., 2004.

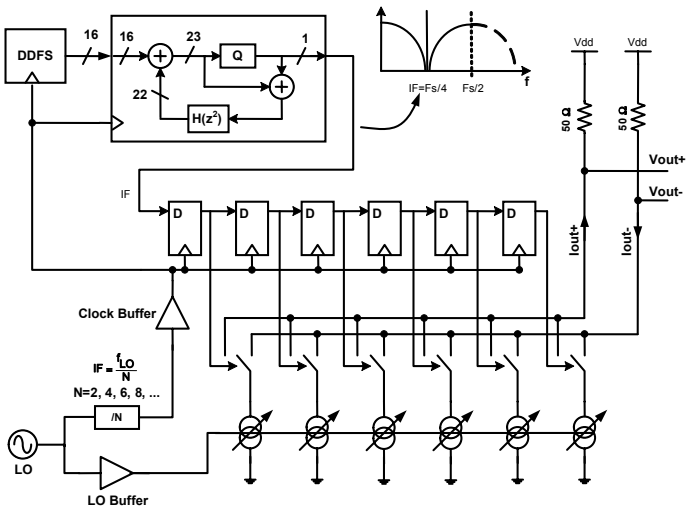

Figure 31.7.1: Block diagram of the RF FIR-DAC with 6-tap reconstruction filters.

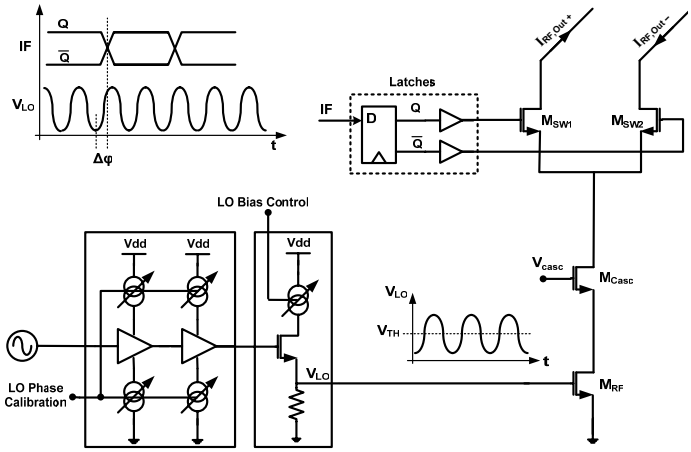

Figure 31.7.2: Cascode unit current source with adjustable LO driver, IF switches, and switch drivers.

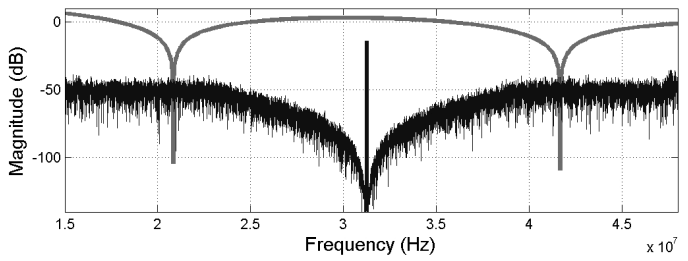

Figure 31.7.3: Frequency response of the 6-tap FIR filter and $f_s/4$ bandpass $\Delta\Sigma$ noise shaper for f_s=125MHz, where f_s is the IF signal sampling frequency.

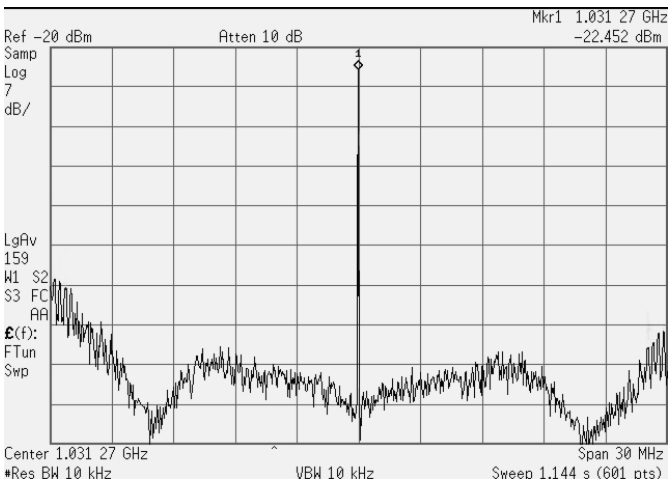

Figure 31.7.4: The spectrum of the FIR-DAC output up-converted to RF.

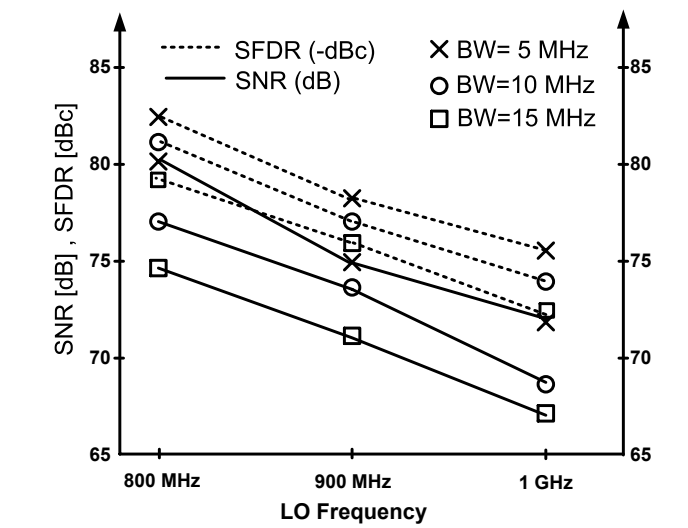

Figure 31.7.5: SFDR and SNR measured at 3 different LO frequencies for different bandwidths, where $f_{IF}=f_s/4$.

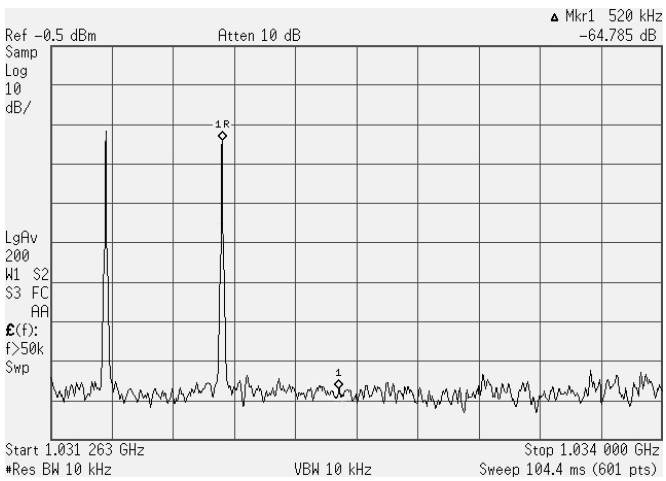

Figure 31.7.6: Measured dual-tone spectrum for the RF DAC for f_{LO}=1GHz, f_s=125MHz, f_1=31.5MHz, and f_2=32.2MHz.

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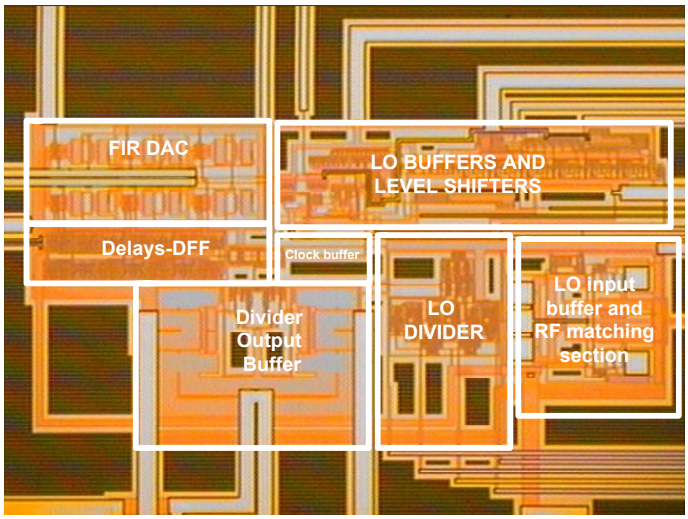

Figure 31.7.7: Die micrograph of the RF DAC.

